Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A bridge for a Host-Bridge-Device system, the bridge comprising:

at lease one bridge chip for controlling operations of the bridge; and

one corresponding activation circuit for each bridge chip, each activation circuit disabling the corresponding bridge chip after a power-on, a hardware reset, or physical disconnection from the host and enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal.

[c2] 2. The bridge of claim 1 wherein the predetermined protocol initialization signal is a signal showing a physical connection between the host and the bridge has been built, a signal from the host to reset the bridge/device, a signal from the host to initialize the bridge/device, or a signal from the host to acknowledge the existence of the bridge/device.

[c3] 3. The bridge of claim 1 wherein each bridge chip comprises the corresponding activation circuit.

[c4] 4. The bridge of claim 1 wherein when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface.

[c5] 5. The bridge of claim 1 wherein when the bridge chip is enabled, the enabled bridge chip drives all pins of a device bus interface connecting the device bus interface to the enabled bridge chip so that the enabled bridge chip controls the device bus interface.

[c6] 6. The bridge of claim 5 wherein when the bridge chip is enabled, the enabled bridge chip retains control of the device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host.

[c7] 7. A device comprising the bridge of claim 1.

[c8] 8. A device comprising:
a bridge for allowing communications between the device and a host computer system, the bridge comprising:
at least one bridge chip for controlling operations of the bridge; and
one corresponding activation circuit for each bridge chip, each activation circuit capable of disabling the corre-

sponding bridge chip upon a power-on, a hardware reset, or a physical disconnection from the host and capable of enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal.

[c9] 9. The device of claim 8 wherein the predetermined protocol initialization signal is a signal showing a physical connection between the host and the bridge has been built, a signal from the host to reset the bridge/device, a signal from the host to initialize the bridge/device, or a signal from the host to acknowledge the existence of the bridge/device.

[c10] 10. The device of claim 8 wherein when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface.

[c11] 11. The device of claim 8 wherein when the bridge chip is enabled, the enabled bridge chip drives all pins of a device bus interface connecting the device bus interface to the enabled bridge chip so that the enabled bridge chip controls the device bus interface.

[c12] 12. The device of claim 8 further comprising an original bus interface capable of communications between the

device and the host computer system utilizing an original bus interface when all of the bridge chips are disabled.

[c13] 13. A method of function activating on a bridge system, the bridge system comprising at least one bridge chip for controlling operations of the bridge, the method comprising:
disabling each of the bridge chips when a power-on or a hardware reset occurs, or when the bridge chip has been physically disconnected from a host;
issuing a predetermined protocol initialization signal to only one of the disabled bridge chips; and
enabling only the bridge chip that received the predetermined protocol initialization signal.

[c14] 14. The method of claim 13 wherein when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface.

[c15] 15. The method of claim 13 wherein when the bridge chip is enabled, the enabled bridge chip drives all pins of a device bus interface connecting the device bus interface to the enabled bridge chip so that the enabled bridge chip controls the device bus interface.

[c16] 16. The method of claim 15 wherein when the bridge chip is enabled, the enabled bridge chip retains control of a device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host.

[c17] 17. The method of claim 13 wherein the predetermined protocol initialization signal is a signal showing a physical connection between a host and the bridge has been built, a signal from the host to reset the bridge or a device connected to the bridge, a signal from the host to initialize the bridge/device, or a signal from the host to acknowledge the existence of the bridge/device.

[c18] 18. A bridge chip comprising:
an activation circuit capable of disabling the bridge chip after a power-on, a hardware reset, or the bridge chip has been physically disconnected from a host, and capable of enabling the bridge chip upon reception of a predetermined protocol initialization signal.

[c19] 19. The bridge chip of claim 18 wherein the predetermined protocol initialization signal is a signal showing a physical connection between a host and a bridge comprising the bridge chip has been built, a signal from the host to reset the bridge or a device connected to the

bridge, a signal from the host to initialize the bridge/device, or a signal from the host to acknowledge the existence of the bridge/device.

[c20] 20. The bridge chip of claim 18 wherein when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface.

[c21] 21. The bridge chip of claim 18 wherein when the bridge chip is enabled, the enabled bridge chip drives all pins of a device bus interface connecting the device bus interface to the enabled bridge chip so that the enabled bridge chip controls the device bus interface.

[c22] 22. The bridge chip of claim 18 wherein when the bridge chip is enabled, the enabled bridge chip retains control of a device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host.